

**CPT-DA2810 Card**  
**TMS320F2810 DSP Controller Card**  
**Technical Brief**

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## **CPT-DA2810 Manual Revision History**

CARD VERSION 1.0: Initial Board for prototype purposes.

Release 1.0 – Initial Release

CARD VERSION 1.1: Modified to include reset signal on pin 60.

Release 1.1 – Modified to match version 1.1 artwork.

Release 1.2 – Modified ADC pinouts to match artwork.

Release 1.3 – Updated schematic and modified the Addressing Map for the TMS320F2810

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**CPT-DA2810 CONTROLLER BOARD TECHNICAL BRIEF**

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## CPT-DA2810 DSP

### 1.0 Overview of the CPT-DA2810

The CPT-DA2810 is a low cost standardised DSP controller board designed to provide a fully flexible interface between the TMS320F2810 DSP processor and a user customised motherboard. The board has been designed to meet different user interface requirements whilst providing a 4 layer DSP core with basic on-board functionality.

The board is based around a Texas Instruments TMS320F2810PBK DSP, which has been specifically developed for use in digital motor/motion control applications.

The CPT-DA2810 card measures 110mm x 55mm.

On-card facilities include:

- TMS320F2810PBK DSP processor
- 64k x 16 Flash (128k x 16 Flash on TMS320F2811PBK)
- 1k x 16 OTP ROM
- 4k x 16 Boot ROM
  - Software Boot Tables
  - Standard Math Tables
- 18K x 16 Single Access RAM (SARAM) made up of:
  - L0 and L1: 2 Blocks of 4K x 16 Each SARAM
  - H0: 1 Block of 8K x 16 SARAM
  - M0 and M1: 2 Blocks of 1K x 16 Each SARAM
- Serial Flash Memory with 1Mbit of non-volatile storage
- 1 off Power LED
- 2 off indication LEDs
- Reset/Power-On Circuitry
- Power supply to generate all on-card supplies
- Power supply operation from input 5VDC

The card also supports the following peripheral interfaces:

- JTAG interface
- 1 off clocked Serial Peripheral Interface (also enables external Flash reprogramming)
- 1 off 3.3V-TTL serial interface
- 1 off 80-way Connector with:
  - 12 off 12-bit 0-3V ADC inputs
  - 2 off Serial Communications Interfaces
  - 1 off Enhanced Controller Area Network (eCAN)
  - 2 off Event Managers
  - 3 off Interrupts

Figure 1-1 shows a functional block diagram of the CPT-DA2810 card, illustrating all major sections.

CPT-DA2810 CONTROLLER BOARD TECHNICAL BRIEF

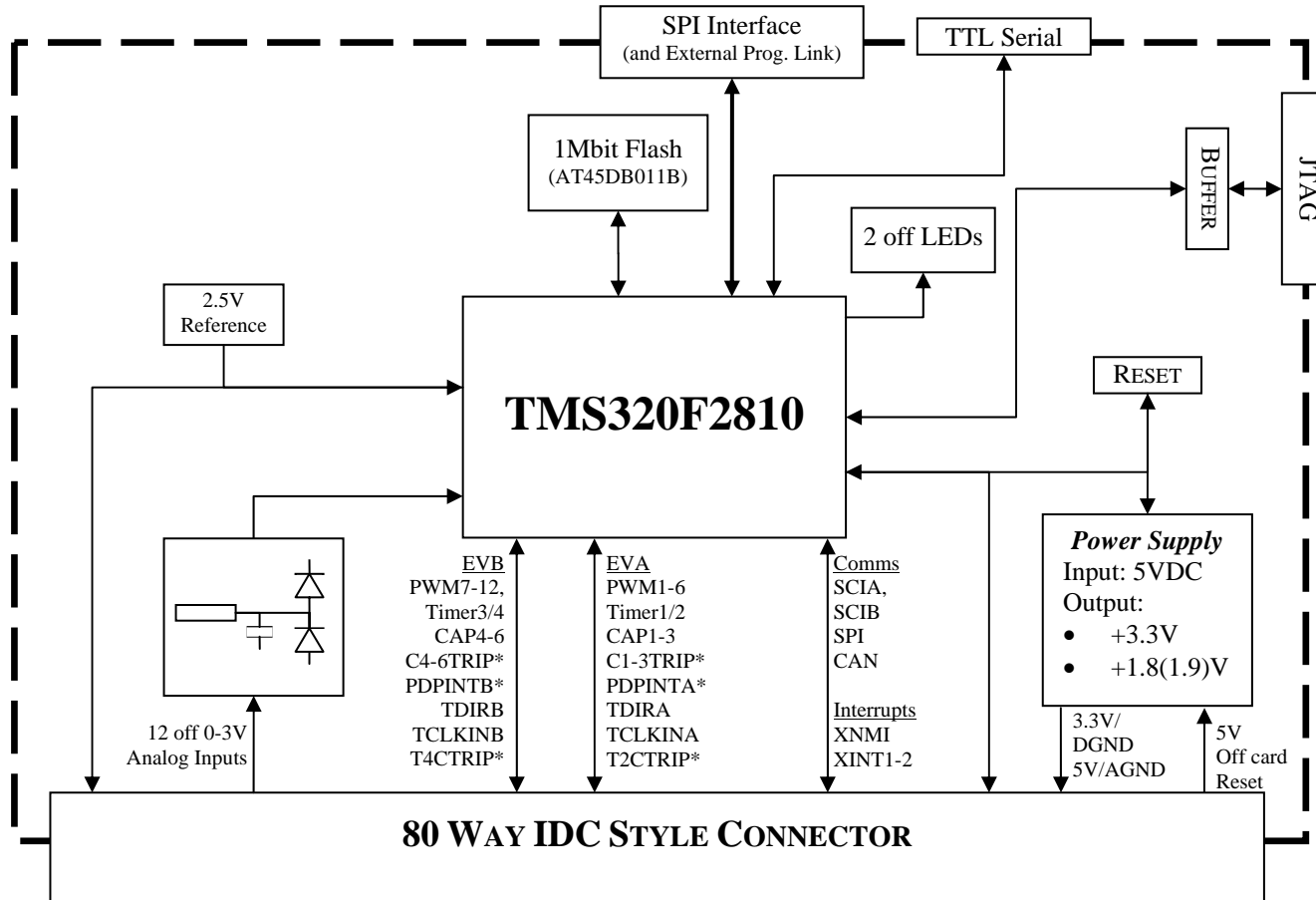


Figure 1-1: Functional Diagram of CPT-DA2810 Controller Board

### 1.1 Digital I/O

The CPT-DA2810 card supports a maximum of 51 bits of 3.3V-TTL digital I/O, depending on the user defined configuration of specific DSP pins. Of these pins, 49 are supplied non-buffered to the main external connector while the remaining 2 are shared with the on-card LEDs and available on the SPI programming connector.

All digital I/O pins on the TMS320F2810 chip have the capability to operate in either “Digital I/O or “Peripheral I/O” mode. The user must select the correct mode of operation for each pin within their software.

### 1.2 Analog Inputs

The TMS320F2810 DSP has 16 off ADC inputs that accept voltages in the range of 0-3V. The analog inputs are divided into two banks of 8 (ADCINA0-7 and ADCINB0-7). Each bank feeds into an 8 to 1 analog multiplexer with a sample and hold circuit. The outputs from the two sample and hold circuits are fed directly into a single 12-bit ADC Module. The ADC module is capable of interleaving ADC conversions between the two banks to achieve a “pipelined” conversion process. This reduces the overall time required for “simultaneous” conversions. The maximum total conversion time for each ADC unit is 80ns (with a 25MHz ADC clock).

The CPT-DA2810 analog inputs are configured to provide 4 off precision reference inputs for self calibration and 12 off filtered external inputs to the TMS320F2810.

The CPT-DA2810 card has on-card precision 2.5V and 1.25V references that should be used for calibration of the internal ADC. Each ADC bank has a 1.25V and 2.5V reference fed to channels 6 and 7 for calibration purposes. It is strongly recommended that the ADC be software calibrated for both gain and offset. Please consult the Texas Instruments documentation on the ADC converter for further information. *TMS320x281x DSP Analog-to-Digital Converter (ADC) Reference Guide*, Literature Number: *SPRU060D*.

The 12 off filtered analog inputs are available on the 80-way header. They each have a low pass or “glitch” filter and a diode clamp circuit before they are fed into the DSP. The board accepts 0-3V inputs for these circuits.

The 2.5V reference is also available on the 80-way header for use off card. It is recommended that this reference be fed into an off-card op-amp circuit for external buffering rather than being used directly.

### 1.3 Gate Drive Interface

The TMS320F2810 DSP supports 16 PWM channel outputs, made up of 6 complementary pairs (12 outputs) with programmable deadbands and 4 independent outputs generated by simple compare functions. The DSP chip has two independent event manager modules and the PWM channels are evenly split between them. Dead band compensation is required to be software-calculated for the simple compare outputs.

Gate fault signals are able to be independently fed back to each event manager via their corresponding PDPINT\* interrupt pin. This enables a DSP hardware interrupt trip to immediately occur on detection of a fault, thus disabling the PWM signals within 12 nanoseconds using hardware logic internal to the DSP.

### 1.4 Communications

The CPT-DA2810 controller board supports two off non-isolated 3.3V-TTL serial communications interfaces (SCI), a 3.3V-TTL synchronous serial peripheral interface (SPI) and a 3.3V-TTL enhanced Controller Area Network (CAN) bus interface.

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The high-speed synchronous serial peripheral interface can be used to communicate to other computer systems. The interface can support either master or slave protocol, selected by software.

The 3.3V-TTL serial port can be used to communicate to a terminal emulation program, via an interface board, to aid in program development.

### 1.5 On-card memory

The CPT-DA2810 controller board supports 64k x 16bit of on-card Flash (128k x 16bit with the TMS320F2811), 18k x 16bit of SARAM and a 4k x 16 Boot ROM. Programs can be directly executed from RAM, via the JTAG interface or from Flash. By default, the card runs programs from the flash memory. Links are provided to enable RAM, SCI or SPI program operation.

In addition to the on-chip memory the CPT-DA2810 has a 1Mbit SPI interfaced Flash Memory chip for external data storage.

### 1.6 Power Supply

The standard CPT-DA2810 controller board has an on-card dual voltage regulator chip that is optimised for operation with Texas Instruments range of TMS320 DSP. The card accepts an input voltage of +5VDC and produces 3.3V I/O and 1.8V/1.9V core voltages.

Analog supplies are generated via an LC filter from the digital 3.3V supply and a precision reference chip is used to produce a stable 2.5V/1.25V for calibration of the DSP analog inputs.

Off card analogs requiring a +5VDC supply should use DVCC supplied from pin 58 to minimise analog grounding loops.

### 1.7 JTAG/programming

The CPT-DA2810 controller board has a JTAG interface for programming the DSP's Flash ROM or RAM. This port can also be used for emulator/debugging purposes using the Code Composer Studio Pod.

## **2.0 Specifications**

### **2.1 Controller DSP Section**

Processor	Texas Instruments TMS320F2810 (optional TMS320F2811)
On-card Memory	64k x 16 Flash Memory (128k x 16 TMS320F2811) 18k x 16 RAM 4k x 16 Boot ROM 1k x 16 OTP ROM
Reset	120ms hardware reset generated on-card from power up and supply failure. Can also be triggered via on-card 2 pin Link ( <b>S1</b> ), or via <b>X5.59</b> on Version 1.1 (or later)
Non-Volatile Memory Storage	1Mbit of memory storage using an SPI flash ROM chip Accessed via SPI interface on DSP
Interrupts	3 off masked external interrupts (XINT1, XINT2, XINT13/NMI) Support for 2 off PDPINT interrupts

### **2.2 Analog Inputs**

Number of Channels	16 single ended	
A/D Resolution	12 bits	
A/D Conversion Time	80ns	
Number of ADC's	1 (8 channels are multiplexed on-chip to form a bank)	
Number of S/H units	2 (each bank has one sample and hold unit)	
Reference Voltages	ADCINA6, ADCINB6	2.5V
	ADCINA7, ADCINB7	1.25V

#### **2.2.1 AC General Inputs**

Definition	12 off 0-3V analog inputs with low pass filter capacitors ADCINA0-5 ADCINB0-5
Input Voltage Range	0-3V maximum
Dynamic Response	Cut-off frequency >150kHz
PCB Connections	80-way IDC header ( <b>X5</b> ) between pins 60 and 80

## 2.3 Digital I/O

### 2.3.1 All Available Digital I/O

Definition	49 bits total GPIOA0-A15, GPIOD0-D1 (shared with Event Manager A) GPIOB0-B15 GPIOD5-D6 (shared with Event Manager B) GPIE0-E2 (shared with interrupts) GPIOF0-F3 (shared with SPI port) GPIOF4-F5 (shared with SCIA port) GPIOF6-F7 (shared with eCAN bus) GPIOG4-G5 (shared with SCIB port)
Digital high input voltage threshold	2.0V
Digital low input voltage threshold	0.8V
Digital outputs rated at	±4mA per bit, ABSOLUTE MAXIMUM ±8mA for GPIOD0
PCB Connection	GPIOF0-F3, F11 & F14 – 10-way IDC header ( <b>X2</b> ) All other I/O available on 80-way IDC header ( <b>X5</b> )

## 2.4 Digital Outputs

Definition	GPIOF11, F14 (shared with on-card LEDs) Note: <b>H1</b> is accessed through Port GPIOF14 <b>H2</b> is accessed through Port GPIOF11 <b>H3</b> is a power LED
Digital outputs rated at	±4mA per bit, ABSOLUTE MAXIMUM
Colours:	All on-card LEDs are GREEN
PCB Connection	GPIOF0-F3, F11 & F14 – 10-way IDC header ( <b>X2</b> )

## 2.5 PWM Gate Drive Interface

Definition	16 PWM Outputs split up over 2 off Event Managers
PWM Outputs per Event Manager	Each event manager has 8 PWM outputs consisting of – 3 independent complementary pairs (6 outputs) with programmable deadband generation 2 gate drive outputs generated from two independent outputs, for which deadband compensation must be implemented in software
Gate Fault Interrupt	PDPINTA* and PDPINTB*, which when unmasked and activated, immediately disable the PWM outputs. Response time is ~12nsec after fault detection The PWM signals are placed into a high impedance state
Output Voltage	0-3V
PCB Connections	80-way IDC header ( <b>X5</b> )

## 2.6 Communications Interface

Definition	The TMS320F22810 has two off serial communications interface ports (SCIA and SCIB), two off serial peripheral interfaces (SPI and McBSP) and an enhanced controller area network port (eCAN)
Configuration	<b>DEFAULT</b> mode is for SCIA and SCIB to be set up as 3.3V-TTL level serial ports and for the SPI to be set up as digital I/O
Isolation	None

### 2.6.1 Serial Communication Interface – SCIA

Definition	Two-wire asynchronous serial port (UART) that supports a 16-level, receive and transmit FIFO for reducing servicing overhead. The receiver and transmitter are double buffered with separate enable and interrupt bits  <b>DEFAULT MODE:</b> 3.3V-TTL level serial connection, providing two pin serial communications for interface to an off-card 3.3V-TTL level to RS-232 translation card. This is necessary for interfacing to a standard PC serial port
Communications Port	SCIA
PCB Connections	4-way pin strip header with VCC and GND connections ( <b>X3</b> ) Also available on 80-way IDC header <b>X5</b> pins 10 (SCITXA) and 11 (SCIRXA)

### 2.6.2 Serial Communication Interface – SCIB

Definition	Two-wire asynchronous serial port (UART) that supports a 16-level, receive and transmit FIFO for reducing servicing overhead. The receiver and transmitter are double buffered with separate enable and interrupt bits  <b>DEFAULT MODE:</b> 3.3V-TTL level serial connection, providing two pin serial communications for interface to an off-card 3.3V-TTL level to RS-232 translation card. This is necessary for interfacing to a standard PC serial port
Communications Port	SCIB
PCB Connections	Available on 80-way IDC header <b>X5</b> pins 12 (SCITXB) and 13 (SCIRXB)

### 2.6.3 Serial Peripheral Interface – SPI

Definition	Four-pin serial peripheral interface (SPI) module. It is a high speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate  <b>DEFAULT MODE:</b> Configured as digital I/O pins
Compatibility	4 wire SPI mode
PCB Connection	10-way IDC connector ( <b>X2</b> ) Also available on 80-way IDC header <b>X5</b> pins 14 (SPISIMO), 15 (SPISOMI), 16 (SPICLK) and 17 (SPISTE*)

### 2.6.4 Enhance Controller Area Network Module – eCAN

Definition	CAN bus module which supports up to 1Mbps transfer
Compatibility	Fully compatible with CAN protocol version 2.0B
PCB Connections	Available on 80-way IDC header <b>X5</b> pins 8 (CANTX) and 9 (CANRX)

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### 2.7 JTAG

Definition	DSP interface connection, which enables the TMS320F2810 to interface to an ICE to provide a real-time debugging environment
Compatibility	Compatible with IEEE 1149.1 standard for scan-based emulation
PCB Connection	14-way IDC connector ( <b>X4</b> )

### 2.8 Software

Standard Support Software	Monitor Program, standard library source code, sample programs Texas Instruments: Code Composer Studio V3 and above
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### 2.9 General

Physical Dimensions	L: 55mm
	W: 110mm
	H: 11mm approx.
Mounting Arrangement	2 off 3.5 mm holes spaced 102mm apart at the top corners of the board 80-way IDC header can also be soldered into the motherboard to provide additional support
Environmental	-40 – 85°C ambient operating temperature 5% - 95% non condensing humidity

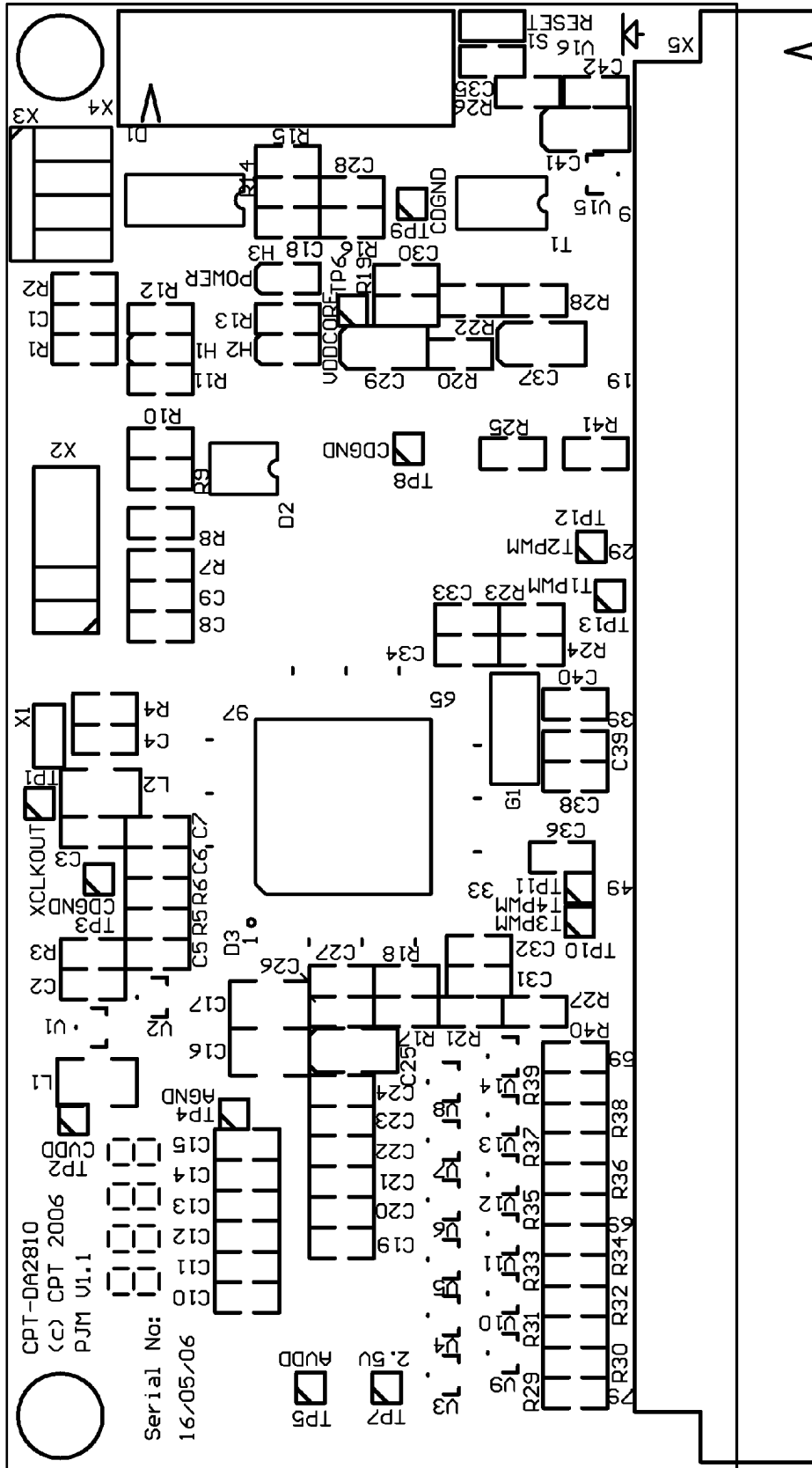
### 2.10 Power Supply

Input Voltage Range	5VDC
Standalone Input Current	<b>100-250mA</b> (depending on the active sections within the DSP)
Max Input Power	Approx. <b>TBD ~500mW</b>
Supplies Generated on-card	+3.3V Digital
	+1.8V (+1.9V) DSP Core
	+2.5V Analog Reference
Input Power Connector	80-way IDC Connector ( <b>X5</b> ) DVCC (+5V) on pins 1-3, DGND on pins 4-6

**Appendices**

Appendix A Component Layout

Top Layer



**Appendix B Link and Test Point Locations**

Top Layer

